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EXAMINER
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ART UNIT	PAPER NUMBER
2664	11

DATE MAILED: 05/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/552,983	Applicant(s) CHRISTIAN, PATRICK	
	Examiner Yvonne Q. Ha	Art Unit 2664	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 March 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,5-9 and 11-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,5-9 and 11-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *#10, 3/4/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The amendment filed on 3/4/2004 has been entered. Claims 1, 5-9 and 11-20 are pending.

Drawings

2. The drawings are objected to because the text labels are missing in figure 1. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 5, 6, and 8, 9, 11-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Trevitt et al. (US Patent 6,510,161) in view of Irwin et al. (US Patent 5,81,771).

Referring to Claims 1, 8, 9, and 11, Trevitt discloses a hardware switching system for transferring received digital data at the incoming ports (Fig. 3, reference 305) and transmitting to outgoing destination from outgoing ports (Fig. 3, reference 305) comprising of a frame transfer controller (i.e. buffer storage address generator and output stage; Fig. 3, reference 310) which provides data and corresponding addresses (Col.6, lines 14-18) and retrieves selected data (Col. 6, lines 23-27) using multiple addresses to access portions of each memory location (Col. 10, lines 66-67; Col. 11, lines 1-67; Col. 12, lines 1-67; Col. 13, lines 1-11) from shared memory (i.e. buffer storage, address storage, indirect addressing mechanism; Fig. 3, reference 330; Fig. 5)

coupled to ports (Col. 5, lines 38-40) which stores the data and addresses to access the data (Col. 5, lines 49-60), and a reader (i.e. address storage address generator; Fig. 4, reference 450) which provides the memory address (Col. 6, lines 23-32). Trevitt failed to teach the buffer storage is organized so each timeslot corresponds to a unique word location in the storage. However, Irwin discloses the synchronization of frame timing of input multiplexer such that a channel (timeslot) buffer memory and a DS0 connection memory are both synchronized to operating rates of incoming and outgoing mux TDM frame buses; buffer memory at a sequential series of memory addresses that match the fame and timeslot order of the incoming frames; the timeslot addresses are sequentially read from the DS0 connection memory and applied to a read address port of DS0 buffer (col. 10, lines 65- col. 11, lines 1-43). At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine the teaching of Trevitt timeslot handling with shared memory with the teaching of Irwin buffer memory of addresses that match the frame and timeslot order of the incoming frames. Both teachings disclose the time switching of incoming data frames with storage or shared memory. In a typical TDM telephone switching facility, the core of switching system consists of a call controller connected with time and space switching elements of a switching matrix. Time switching of frame and time slot organized data words at a rate are faster than operating read/write cycle rate of time switching memory elements. For switching data words occurring in a frame and time slot organized stream, write and read control signals and time control slot signals are required, in which data words are assembled from the input signal stream for storage and time slots.

Referring to Claim 5, Trevitt discloses all aspects of the claimed invention and further teaches a system where the addresses include bits wherein the lower order two bits of each

address are used to identify one of four bytes in a word location in the buffer storage (Col. 11, lines 1-9; Figs. 8A-8C).

Referring to Claim 6, Trevitt discloses all aspects of the claimed invention and further teaches the use of staggering data frames that have been time sliced so that on any clock cycle one memory portion is accessed for writing and on a next clock cycle the memory portion is accessed for reading (Col. 4, lines 3-9; Col. 4, lines 16-19; Col. 4, lines 30-32; Col. 4, lines 45-51).

Referring to Claim 11, Trevitt discloses all aspects of the claimed invention and further teaches the use of timeslot of data in shared memory that is readable in a Fibre Channel switch (Col. 5, lines 29-48).

Referring to Claims 12, 15, Trevitt discloses all aspects of the claimed invention and but failed to teach a number of outgoing timeslots differs from incoming timeslots. However, Irwin discloses a number of outgoing timeslots differs from incoming timeslots (col. 11, lines 11-37). At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine the teaching of Trevitt timeslot handling with shared memory with the teaching of Irwin buffer memory of addresses that match the frame and timeslot order of the incoming frames. Both teachings disclose the time switching of incoming data frames with storage or shared memory. In a typical TDM telephone switching facility, the core of switching system consists of a call controller connected with time and space switching elements of a switching matrix. Time switching of frame and time slot organized data words at a rate are faster than operating read/write cycle rate of time switching memory elements. For switching data words occurring in a frame and time slot organized stream, write and read control signals and time control slot

signals are required, in which data words are assembled from the input signal stream for storage and time slots.

Referring to Claims 13, 16, 19, 20, Trevitt discloses all aspects of the claimed invention but failed to teach data transfer from incoming source to buffer is not synchronized with the data from buffer output. However, Irwin discloses data transfer from incoming source to buffer is not synchronized with the data from buffer output (col. 12, lines 27-67, synchronous and asynchronous modes, figure 6). At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine the teaching of Trevitt timeslot handling with shared memory with the teaching of Irwin buffer memory of addresses that match the frame and timeslot order of the incoming frames. Both teachings disclose the time switching of incoming data frames with storage or shared memory. In a typical TDM telephone switching facility, the core of switching system consists of a call controller connected with time and space switching elements of a switching matrix. Time switching of frame and time slot organized data words at a rate are faster than operating read/write cycle rate of time switching memory elements. For switching data words occurring in a frame and time slot organized stream, write and read control signals and time control slot signals are required, in which data words are assembled from the input signal stream for storage and time slots. The multiplexers supports both synchronous and asynchronous for different types of incoming data.

Referring to Claims 14, 17, Trevitt discloses all aspects of the claimed invention and but failed to teach data transfer from incoming source to buffer is synchronized with the data from buffer output. However, Irwin discloses data transfer from incoming source to buffer is synchronized with the data from buffer output (col. 12, lines 27-67, synchronous and

asynchronous modes, figure 6). At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine the teaching of Trevitt timeslot handling with shared memory with the teaching of Irwin buffer memory of addresses that match the frame and timeslot order of the incoming frames. Both teachings disclose the time switching of incoming data frames with storage or shared memory. In a typical TDM telephone switching facility, the core of switching system consists of a call controller connected with time and space switching elements of a switching matrix. Time switching of frame and time slot organized data words at a rate are faster than operating read/write cycle rate of time switching memory elements. For switching data words occurring in a frame and time slot organized stream, write and read control signals and time control slot signals are required, in which data words are assembled from the input signal stream for storage and time slots. The multiplexers supports both synchronous and asynchronous for different types of incoming data.

5. Claim 7 is rejected under 35 U.S.C 103(a) as being unpatentable over Trevitt et al. (US Patent 6,510,161) in view of in view of Irwin et al. (US Patent 5,81,771) and in further view of Sakamoto et al. (US Patent 6,185,212).

Referring to Claim 7, Trevitt and Irwin disclose a system where free and random addresses stored are used to identify portions of data are stored in one or more locations but failed to disclose consecutive addresses in storage (Figs. 7, 8A, 8B). However, Sakamoto discloses DRAM is the fastest consecutive access when performing the data writing and reading operation by using consecutive column access, such as the consecutive address read and write operation (col. 2, lines 39-50). At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine the teaching of Trevitt timeslot handling with

shared memory using free and random addresses with Sakamoto teaching of managing multiple queues in a common RAM or link list where each data element in a particular queue includes a pointer to the next consecutive element in the queue. One of ordinary skill in the art would have been motivated to combine the teaching of Trevitt timeslot handling with shared memory using free and random addresses with Sakamoto teaching of use of consecutive address read/write written into a memory system because it simplifies the algorithm used by the reader which provides the memory addresses for data reconstruction from multiple timeslots stored in the shared memory.

Response to Arguments

6. Applicant's arguments with respect to claims 1, 5-9 and 11-20 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a). A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yvonne Q. Ha whose telephone number is 703-305-8392. The examiner can normally be reached on Monday-Friday 7a.m.-4p.m. Eastern.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ajit Patel can be reached on 703-308-5347. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

YQH

Ajit Patel
Primary Examiner